Static noise analysis for digital integrated circuits in partially-depleted silicon-on-insulator technology

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↑ ABSTRACT

In this paper, we extend transistor-level static noise analysis tools to consider the unique features of partially-depleted silicon-on-insulator (PD-SOI) technology: floating-body-induced threshold voltage variations and parasitic bipolar leakage currents. This involves a unique state-diagram abstraction of the device physics determining the body-potential of PD-SOI FETs. Based on this picture, a simple model of the body voltage is derived which takes into account modest knowledge of which nets have dependable, regular switching activity. Results are presented using a commericial static noise analysis tool incorporating these extensions.

↑ REFERENCES

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↑ INDEX TERMS

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1 Static noise analysis for digital integrated circuits in partially-depleted silicon-on-insulator technology
Kenneth L. Shepard, Dae-Jin Kim
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In this paper, we extend transistor-level static noise analysis tools to consider the unique features (partially-depleted silicon-on-insulator (PD-SOI) technology: floating-body-induced threshold voltag(variations and parasitic bipolar leakage currents. This involves a unique state-diagram abstraction (the device physics determining the body-potential of PD-SOI FETs. Based on this picture, a simple model of the body voltage is derived which takes into account modest knowledge of which ...

2 Efficient crosstalk noise modeling using aggressor and tree reductions
Li Ding, David Blaauw, Pinaki Mazumder
November 2002 **Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design**
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This paper describes a fast method to estimate crosstalk noise in the presence of multiple aggresso nets for use in physical design automation tools. Since noise estimation is often part of the innerloc of optimization algorithms, very efficient closed-form solutions are needed. Previous approaches have typically used simple lumped 3--4 node circuit templates. One aggressor net is modeled at a time assuming that the coupling capacitances to all quiet aggressor nets are grounded. They also mode ...

3 Circuit effects in static timing: Timed pattern generation for noise-on-delay calculation
Seung Hoon Choi, Kaushik Roy, Florentin Dartu
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Computing the noise on delay effects is required for all circuits from simple ASIC designs to microprocessors. Transistor-level simulation engines make accurate delay calculation affordable onl if the number of simulation per stage is very small. We propose a solution that predicts the alignment of aggressor signals with respect to the victim signal to induce the worst-case noise effe(on delay. The aggressor alignment can be used to setup a detailed simulation. The worst-case dela' in the pre ...

4 Multi-center congestion estimation and minimization during placement
Maogang Wang, Xiaojian Yang, Kenneth Eguro, Majid Sarrafzadeh
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5 Towards true crosstalk noise analysis
Pinhong Chen, Kurt Keutzer
November 1999 **Proceedings of the 1999 IEEE/ACM international conference on Computer-aided design**
Full text available: pdf(123.25 KB) Additional Information: full citation, abstract, references, citings, index terms

Accurate noise analysis is currently of significant concern to high-performance designs, and the number of signals susceptible to noise effects will certainly increase in smaller process geometries. Our approach uses a combination of temporal and functional information to eliminate false transitio combinations and thereby overcome insufficiencies in static noise analysis. A similar idea arises in timing analysis where functional and timing information is used to eliminate false paths. The ...

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Static Noise Analysis for Digital Integrated Circuits in Partially-Depleted Silicon-On-Insulator Technology *

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Abstract

In this paper, we extend transistor-level static noise analysis tools to consider the unique features of partially-depleted silicon-on-insulator (PD-SOI) technology: floating-body-induced threshold voltage variations and parasitic bipolar leakage currents. This involves a unique state-diagram abstraction of the device physics determining the body-potential of PD-SOI FETs. Based on this picture, a simple model of the body voltage is derived which takes into account modest knowledge of which nets have dependable, regular switching activity. Results are presented using a commericial static noise analysis tool incorporating these extensions.

1 Introduction

Partially-depleted silicon-on-insulator (PD-SOI) has emerged as a leading technology for high-performance, low-power deep-submicron digital integrated circuits[1, 2, 3, 4]. PD-SOI technology delivers two main advantages for digital applications: the reduction of the parasitic capacitance associated with source and drain diffusions and the reduction of the reverse-body effect in FET series connections. Acting together, these effects result in the faster switching of stack structures in PD-SOI than in bulk CMOS. In addition to higher speed (or lower power) operation, PD-SOI also enables the possibility of greater logic function from a given channel-connected component (CCC).

The reduced reverse-body effect in stack structures comes about because the body of the transistors is floating. At the device and circuit level, however, this floating-body effect poses major challenges in the successful use of this technology. There is a parasitic bipolar effect which can result in noise failures if not correctly considered[5]. In addition, there can be large "uncertainties" in the body potential, and consequently the threshold voltage, of devices due to unknown past switching activity. Without special effort, the design margining required in timing analysis to protect against this uncertainty erodes all of the potential performance advantage under nominal operation. Similarly, without special effort in noise analysis, many circuit styles in which noise margin is strongly determined by threshold voltage (e. g. dynamic circuits) could be significantly overdesigned because of conservative body-voltage margining. Static timing[6] and static noise[7] analysis tools, which have become central to the verification of leading-edge digital designs, must be enhanced to understand the unique features of SOI technology. In particular, they must provide accurate bounds on the floating-body potentials of the devices from known switching and circuit topology information. Where these bounds are not adequate to prevent overdesign, they should provide options for reducing the potential body voltage variation.

In this paper, we work with BSIM3SOI[8] models for an IBM partially-depleted SOI technology described elsewhere[9]. Devices have a $0.25\mu m$ effective channel length, $5-nm$ gate oxide, $350-nm$ buried oxide, and $140-nm$ thin silicon film.[1] While the detailed results we present here apply to this technology, the techniques are generally applicable to any PD-SOI technology.

Reference [10] presents techniques for body voltage estimation in PD-SOI circuits and applies them to transistor-level static timing analysis. Reference [7] considers the techniques and methods of transistor-level static noise analysis. In this paper, we combine these approaches to consider the unique issues of static noise analysis for PD-SOI circuits. In Section 2, we review the device physics determining the body voltage and parasitic bipolar effects. We do this from the perspective of the circuit-centric state-diagram abstraction introduced in Reference [10]. We next consider possible approaches for body voltage estimation and settle on one approach that seems most suitable for static noise analysis. In Section 3, we review the essentials of transistor-level static noise analysis. Furthermore, we consider the special issues associated with static noise analysis in PD-SOI. In Section 4, we consider these techniques applied in an SOI-aware prototype of a commercial static noise analysis engine. Section 5 offers conclusions and directions for future work.

2 PD-SOI device physics

The body potential of a PD-SOI FET is determined by capacitive coupling of the body to the gate, source, and drain, by diode currents at the source-body and drain-body junctions [including gate-induced drain leakage (GIDL)[11]], and by impact ionization currents produced by current flow through the device (sometimes referred to as the on-state impact ionization current). Moreover, it is convenient to distinguish "fast" and "slow" processes. Fast processes can change the body potential on time scales on the order of or less than the cycle time, while slow processes require time scales much longer than the cycle time (up to milliseconds) to affect the body voltage. There are two fast mechanisms at work: switching transitions on the gate, source, or drain which are capacitively coupled to the body (which we call *coupling displacements*), and forward-bias diode currents across source-body and drain-body junctions with voltages exceeding the diode turn-on voltage (which we call *body discharge*). The slow processes involve charging or discharging the body through reverse-biased or very weakly forward-biased diode junctions and through impact ionization.

As a (usually) dynamic circuit node, the floating body has "memory." To model the switching history determining the body voltage

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[1] We modified the device parameters of the model slightly to reduce the impact ionization current at 2.5-V supply. They, therefore, differ slightly from those used in Reference [10].

of a particular device, we use the state diagram abstraction shown in Figure 1. (This diagram applies to the nFET. The state diagram of the pFET is the "dual" of this, in which the gate is high rather than low in states 3, 4, and 5; and low rather than high in states 1, 2, and 6.) The states denoted with solid circles represent "static" states, states in which the FET can be stable, in constrast with the "dynamic" states 6a and 6b, which are only present transiently during switching events. For example, state 1 corresponds to the case in which the gate is high and both the source and drain are low. Arrows indicate possible state transitions produced by switching events in the circuits containing these FETs. If the device is allowed to remain in one state for a very long time, the body voltage in each state i will achieve a dc value, denoted as s_i.

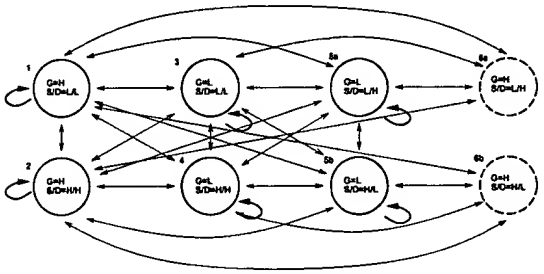

Figure 1: State diagram for a PD-SOI nFET.

We can represent the charge stored on the body as the value of the body voltage in one particular state of Figure 1, the *reference state*, which we choose to be state 2 for the nFET and state 1 for the pFET. From this reference body voltage (V_B^{ref}), we can then determine the corresponding body voltage in each state i (V_B^i) according to:

$$V_B^i = V_B^{ref} + d_i(V_B^{ref})$$

The displacements, $d_i(V_B^{ref})$, are explicitly shown to be dependent on the reference body voltage because of the strong voltage-dependence of the capacitances of the source-body, drain-body, and gate-body.

With the reference body voltage as a "state-independent" way of representing the charge trapped on the body, we proceed to characterize each state i in Figure 1 by two values of this reference voltage, V_i^{zero} and $V_i^{forward}$. V_i^{zero} represents the steady-state value of the reference body voltage, achieved by remaining in state i for a long time. This follows immediately from the s_i in each state.

$$s_i = V_i^{zero} + d_i(V_i^{zero}) \quad (1)$$

$V_i^{forward}$ represents the value of the reference body voltage for the nFET (pFET) to which the body would be very quickly pulled down (up) as a result of body discharge (charge), if state i were accessed with a higher (lower) reference body voltage than $V_i^{forward}$. These $V_i^{forward}$ values presume that the fast body discharge will bring the forward-biased-junction bias down to a turn-on voltage of 0.6 V. (It is important to note that fast body discharge can trigger parasitic bipolar leakage between source and drain for FETs in state 5.) In our example technology at 2.5 V, for instance, this means that if a FET which reached a dc steady-state in state 4 (with a V_4^{zero} of 3.43 V) switches into state 2, the reference body voltage will quickly discharge to $V_2^{forward} = 3.1V$. If the FET subsequently remains in state 2 for a long time, V_B^{ref} will eventually decrease to $V_2^{zero} = 2.5V$.

Reference [10] uses this information to provide two modes of body voltage "estimation." In "full-uncertainty" analysis, we assume that we have no knowledge of the switching activity of the circuit. We must choose maximum and minimum possible values of the body voltage that cover all possible stimulus and history. We say that a state is *accessible* if the circuit topology allows the state to be visited. (For example, for the nFET of an inverter, those states with the source high would not be accessible, because the source of the nFET is tied to ground.) We let $\mathcal{A}$ represent the set of such accessible states, including possibly the dynamic state 6. In this case, the minimum and maximum body voltages are given by:

$$(V_B^{ref})_{max} = \max_{j \in \mathcal{A}} V_j^{zero} \quad (2)$$

$$(V_B^{ref})_{min} = \min_{j \in \mathcal{A}} V_j^{zero} \quad (3)$$

If, however, one is assured that every accessible state is visited with reasonable frequency (i. e., on a time scale that is faster than the "slow" body-voltage mechanism), then the $V_j^{forward}$ values for the nFET (pFET) will cap the maximum (minimum) possible value of the body voltage. This is referred to as "accessibility" body-voltage estimation. For the nFET,

$$(V_B^{ref})_{min} = \min_{j \in \mathcal{A}} V_j^{zero} \quad (4)$$

$$(V_B^{ref})_{max} = \min(\max_{j \in \mathcal{A}} V_j^{zero}, \min_{j \in \mathcal{A}_{static}} V_j^{forward}) \quad (5)$$

while for the pFET,

$$(V_B^{ref})_{min} = \max(\min_{j \in \mathcal{A}} V_j^{zero}, \max_{j \in \mathcal{A}_{static}} V_j^{forward}) \quad (6)$$

$$(V_B^{ref})_{max} = \max_{j \in \mathcal{A}} V_j^{zero} \quad (7)$$

where $\mathcal{A}_{static}$ is the set of all accessible *static* states (i. e. states 1 through 5). State 6 is not included in this "accessibility" analysis because it is visited only "quickly" during a transition and cannot be assured to be active long enough to complete a discharge. Reference [10] shows how it is possible to refine this estimate even further with stochastic techniques. These require more detailed knowledge of signal timing and probabilities, which are difficult to obtain and assure in the context of noise analysis.

While accessibility analysis does not require detailed switching knowledge, it does require that there is enough switching activity that every accessible state is visited with a minimum frequency. At times, this, too, may be difficult to ensure. We, therefore, propose a *modified accessibility analysis* that we will apply in the context of static noise analysis. In this approach, signals in the design can be marked as *active*. This means that these particular signals are assured to switch with regular frequency. The clock net is one immediately obvious active net. We then use these active net tags to come up with a set of constraints that must be satisfied by a modified accessibility set of states $\mathcal{A}_{ma}$. The body voltage will then be determined by equations identical to those used for accessibility analysis except that $\mathcal{A}_{static}$ is replaced by $\mathcal{A}_{ma}$. $\mathcal{A}_{ma}$ will be the accessibility set for the nFET (pFET) which satisfies the contraints while ensuring the maximum (minimum) value of the body voltage. These constraints are derived from the following rules:

- If the gate of the FET is an active net, then there must be a state in $\mathcal{A}_{ma}$ with the gate high and a state in $\mathcal{A}_{ma}$ with the gate low.
- If the source of the FET is connected to ground (supply) through a succession of transistors all of whose gates are active nets, then $\mathcal{A}_{ma}$ must contain a state with the source low (high).
- If the drain of the FET is connected to ground (supply) through a succession of transistors all of whose gates are active nets, then $\mathcal{A}_{ma}$ must contain a state with the drain low (high).

- Same-signal correlations must be considered and can result in stronger constraints. For example, if the gate of the current FET is marked as an active net, but must be high for a path to ground from the source to be present through a path of active-gate FETs, then $\mathcal{A}_{ma}$ must contain a state in which both the gate is high and the source is low.

3 Static noise analysis

References [12, 7] introduce the idea of transistor-level static noise analysis as a key technology for verifying the functionality of large digital integrated circuits in the presence of noise. The approach involves decomposing the design into a collection of channel-connected components (CCCs), transistors that are connected together through their sources and drains. The maximum noise that is possible on each net is calculated as a time-domain waveshape. This worst-case noise considers all significant noise sources: leakage, charge-sharing noise, coupling though the interconnect, and power-supply noise. This is done with a careful choice of vectors on the driving CCCs, referred to as the *sensitization*, which produces this worst case noise. Noise can also propagate from CCC-input to CCC-output (*propagated noise*). Noise failures are determined by the *noise stability*, a type of AC noise margin analysis, of each CCC given the worst case noise appearing at its inputs. This involves calculating the transient sensitivity of the output noise with respect to the dc-level of the input noise. In this paper, we wish to consider only the special considerations associated with applying static noise analysis to PD-SOI circuits and refer the reader to Reference [7] for more details on static noise analysis generally.

There are two important considerations for static noise analysis for PD-SOI circuits. The first is that all of the body voltages must be initialized as part of the CCC analysis used to calculate the noise on each node as well as the CCC analysis used to determine the noise stability of the gate. These body voltages are calculated using the modified accessibility analysis described in Section 2. The approach here is straightforward and depends on the noise type being calculated. Following Reference [10], we calculate two types of noise on each CCC output, V_H noise, which is noise that pulls the output down from the supply level and V_L noise, which is noise that pulls the output up from ground. When calculating V_H noise on a CCC output (or when verifying noise stability in the case that V_H noise is introduced at the output), all of the devices in the pull-down stack are initialized to maximize the device strength by minimizing threshold voltages (maximum body voltages for nFETs and minimum body voltages for pFETs). This increases the strength of these devices in introducing noise. Similarly, all the devices in the pull-up paths are initialized to minimize device strengths by maximizing threshold voltages (maximum body voltages for pFETs and minimum body voltages for nFETs). This reduces the strength of these devices in maintaining the output at the logic high level. For V_L noise, the situation is just the opposite.

The second important consideration in the static noise analysis of PD-SOI circuits is that in calculating both propagated noise and in verifying noise stability, a parasitic bipolar leakage current may also be activated. Because of this, to achieve the worst-case, we must vary the arrival time of the input noise to maximize the output noise; that is, make sure that the noise introduced by parasitic bipolar leakage is superimposing maximally with the propagated noise.

4 Results

We have applied these enhancements to a prototype version of a commercial static noise analysis engine, already being applied to industrial designs in bulk CMOS. We focus our results on the small example shown in Figure 2, where we can tractably validate our results with dynamic simulation. We choose a domino gate with a full latch so that the condition for functional failure is unambiguous (the latch flips). The example, however, illustrates most of the noise analysis issues unique to PD-SOI. Internally, the static noise analysis engine uses a CCC decomposition of this circuit in which the output inverter is partitioned out. In this partitioned circuit, we refer to the dynamic node as *dyns* and the output of the inverter as *outs*.

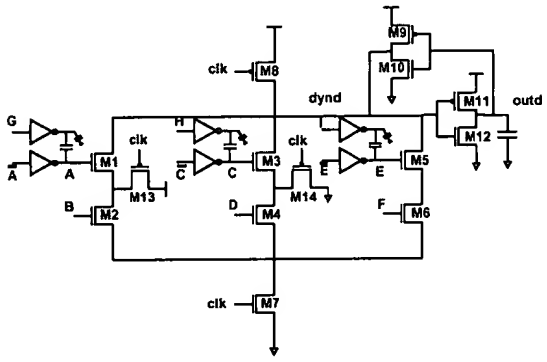

Figure 2: Example circuit.

We intend to compare our static noise analysis results with dynamic simulation of the same circuit by vectors which correspond to the "worst-case" behavior detected in the static analysis. In the circuit of Figure 2, we consider coupling noise that we introduce by the switching of an aggressor (G, H, or I) capacitively coupled to inputs A, C, and E after a long period of switching history, which we call the *prelude*. We consider three different preludes as shown in Table 1. The clock period is $10nsec$ and the prelude is simulated for $100\mu sec$ (so that the body has reached steady state) before the noise is applied. For the purposes of the dynamic simulation, a net that is active during the prelude has a $0 \rightarrow 1$ transition at the middle of the evaluate cycle, every other evaluate cycle. After the prelude, which is different depending on the case considered, the "noise condition" shown in Table 2 is applied, introducing V_L coupling noise on node A for case 1, node C for case 2, and node E for cases 3 and 4. This "noise condition" is identical to the one established by static noise analysis to produce the worst-case V_H noise on node *dynd* in each case. However, instead of a full prelude simulation, in the static analysis, the body voltages of each FET is initialized by the tool with the maximum or minimum value as determined by modified accessibility analysis. The inputs noted as active in Table 1 (in addition to the clock) are considered as active nets in this analysis. In Case 1, a significant parasitic bipolar current is also present; as a result, the tool adjusts the arrival time of the noise on A to produce the maximum peak noise at *dyns*. Cases 1 and 3 yield noise failures, which are correctly predicted by static noise analysis (by sensitivities exceeding one in magnitude for the output inverter – *dyns* to *outs*), while cases 2 and 4 do not.

The noise characteristics are most strongly affected by the body voltages on FETs $M1$, $M3$, and $M5$. The actual (from dynamic simulation) and estimated maximum values (from the static noise analysis tool) for these body voltages are compared in Table 3. In Case 1, transistor $M13$ charges the internal node between transistors $M1$ and $M2$ to V_{DD} every precharge phase. This configuration would be common in bulk CMOS to mitigate charge-sharing noise but is potentially disastrous for SOI since it can allow the body of $M1$ to easily charge to a very high bias. This leave $M1$ with poor immunity to noise on its gate and also leave it preconditioned for parasitic bipolar leakage. Both contribute to the failure in this case. Case 3 is similar, but the fact that net E is under steady switching

Prelude	Node disposition					
	A	B	C	D	E	F
1	0	0	0	0	active	0
2	0	0	active	0	0	0
3	0	0	0	0	active	active

Table 1: The switching conditions of the "prelude," applied for $100\mu sec$ before the noise event to establish steady-state body voltages.

Case	Prelude	A	B	C	D	E	F	G	H	I
1	1	0	1	0	0	0	0	fall	1	1
2	2	0	0	0	1	0	0	1	fall	1
3	1	0	0	0	0	0	1	1	1	fall
4	3	0	0	0	0	0	1	1	1	fall

Table 2: Four noise conditions considered.

means that both states 2 and 4 are accessible for FET $M5$. State 2 accessibility limits the maximum body voltage possible but is not enough to prevent failure. In Case 2, transistor $M14$ discharges the internal node between transistors $M3$ and $M4$ every cycle. From the point of view of our modified accessibility analysis, this is equivalent to Case 4, in which both E and F are active. In both cases, our upper bound is about 250 mV too high, although we correctly predict functionality in the static noise analysis. The main reason for this discrepancy is the neglect of state 6 which is exerting a downward pressure on the body voltage which is not considered in the modified accessibility analysis.

In Figure 3, we show the waveforms associated with the Case 3 failure. Figure 3(a) shows the dynamic simulation of the failure as manifest in the switching of $dynd$ and $outd$. E labels the coupled noise on the gate of $M5$. Figure 3(b) shows the waveform calculated internally in the static noise analysis for nodes $dyns$, $outs$, and E. The diamond on the left axis corresponds to the "initial condition" body voltage applied to transistor $M5$ for the simulation determining the waveform at $dyns$. [Note that $dyns$ does not "switch" because the feedback loop is broken in the CCC decomposition.] Figure 3(c) shows the $dyns$-$outs$ transient sensitivity that is used to detect the failure.

5 Conclusions

We have described extensions to transistor-level static noise analysis to handle the unique issues of PD-SOI technology: floating-body-induced threshold voltage variations and parasitic bipolar leakage currents. In particular, we have developed a model for estimating the possible body voltage variation without simulation which takes into account modest knowledge of which nets have dependable, regular switching activity.

Transistor	Actual body voltage (state 5)	Estimated max body voltage (state 5)
M1 for case 1	0.95 V	0.97 V
M3 for case 2	0.05 V	0.255 V
M5 for case 3	0.720 V	0.787 V
M5 for case 4	0.11 V	0.255 V

Table 3: Body voltage comparison between simulation and static noise analysis.

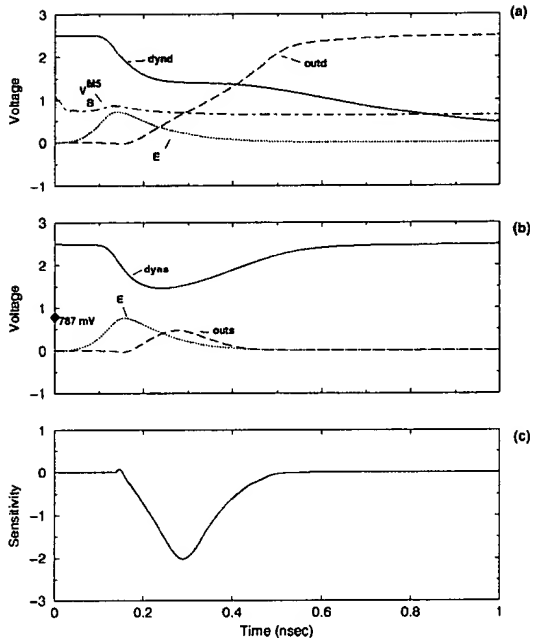

Figure 3: Case 3 results for (a) dynamic simulation and (b) static noise analysis. The sensitivity of the inverter of the dynamic gate to the noise on $dyns$ is shown in (c).

More work is required to include the effects of the dynamic state 6 in modified accessibility analysis. Future work could also include developing techniques by which nets would be explicitly forced active to control body voltage variation. This could be viewed as analogous to DRAM refresh. More work would be required to determine the necessary frequency and nature of this pattern.

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